

FIG. 1

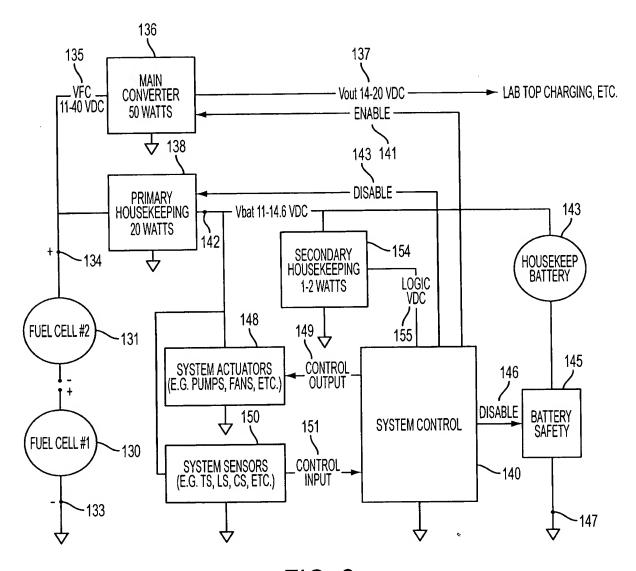


FIG. 2

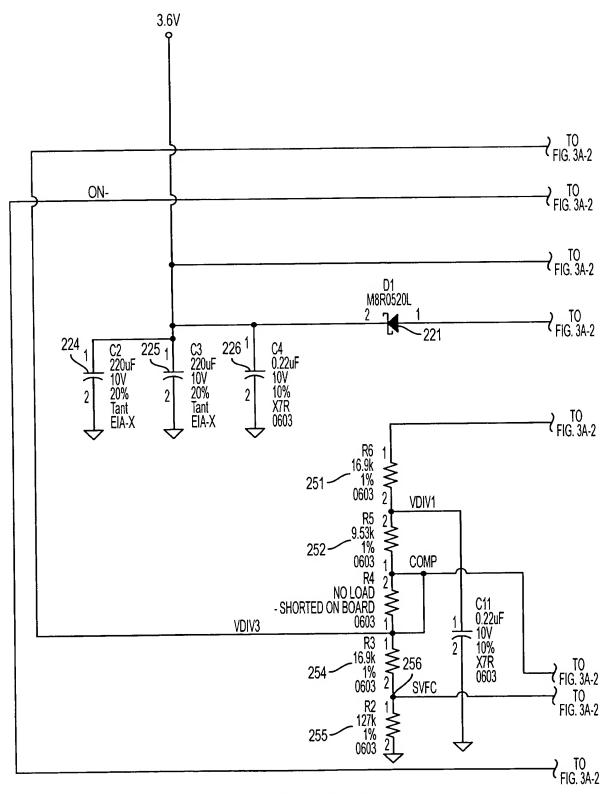


FIG. 3A-1

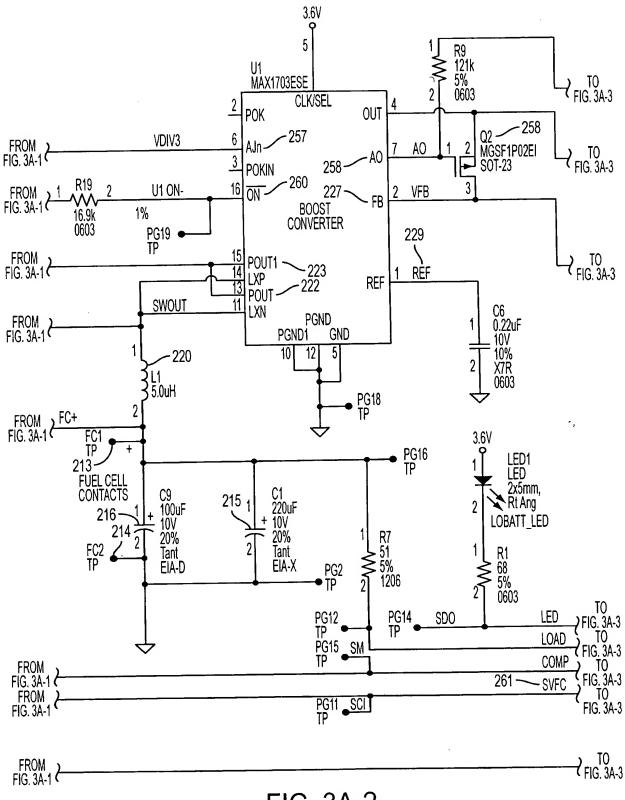


FIG. 3A-2

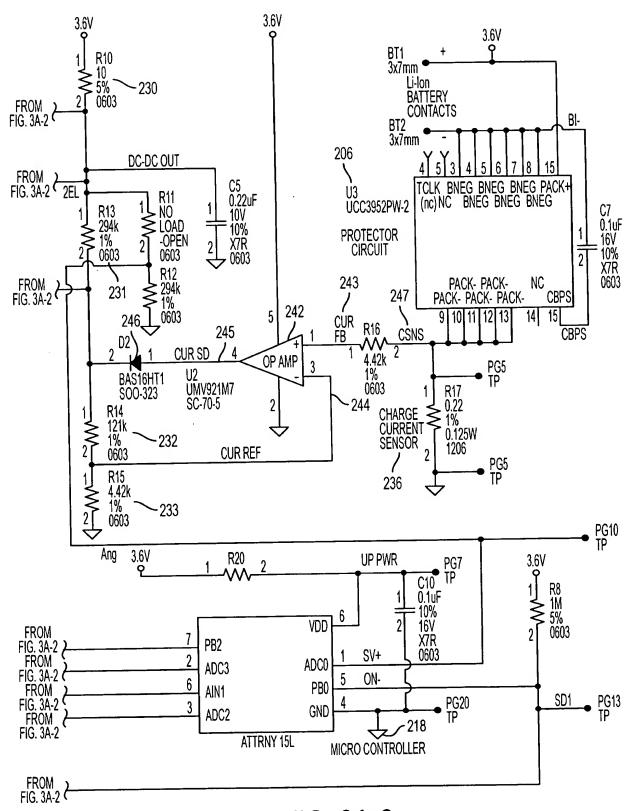


FIG. 3A-3

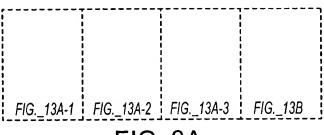


FIG. 3A

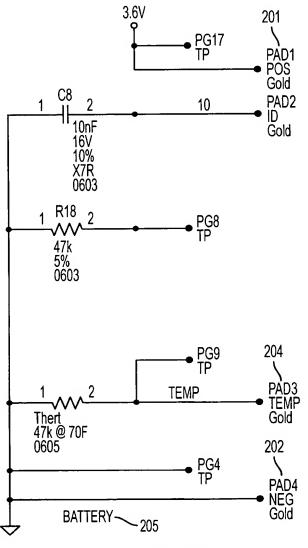
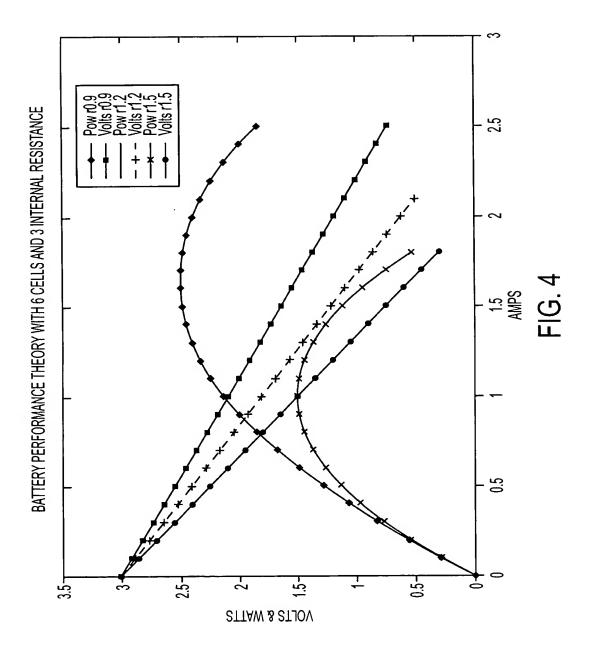
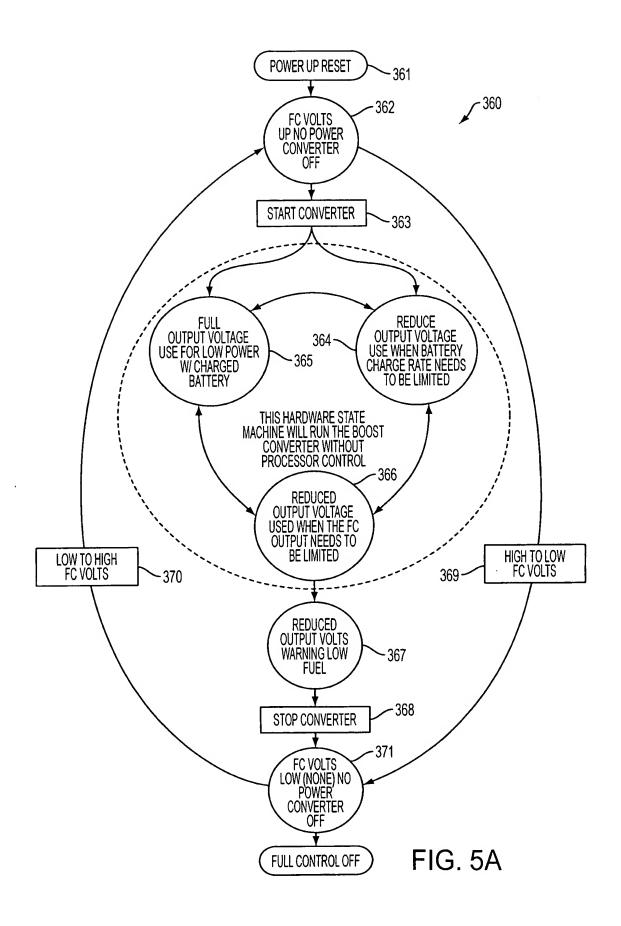


FIG. 3B





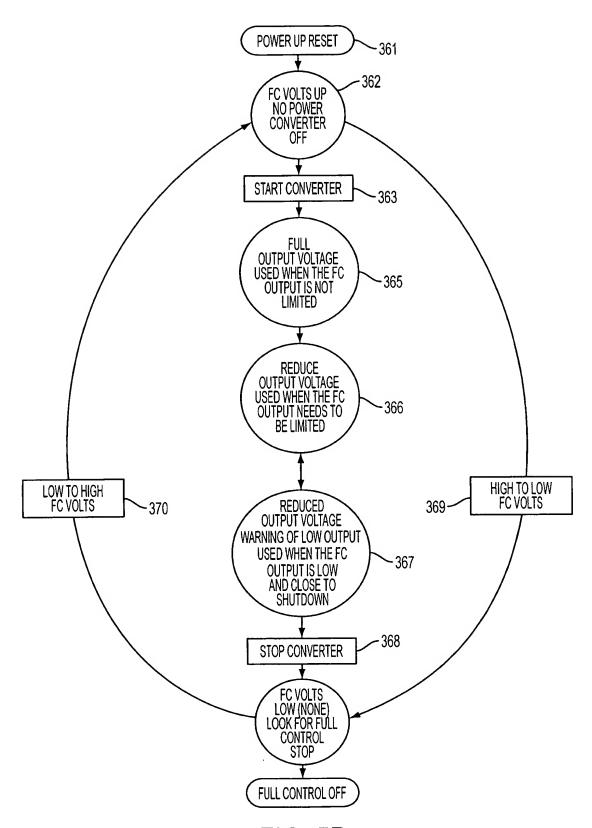


FIG. 5B

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SOFTWARE VFC LEVELS

LEVEL 1 - 2.4V IF OFF LOAD TEST ABOVE, WITH WARNING LEVEL 2 - 1.5V IF ON SLEEP ABOVE
LEVEL 3 - 1.2V IF ON WARNING BELOW
LEVEL 4 - 1.1V IF ON STOP BELOW

HARDWARE TRIP FROM SLEEP IS BETWEEN L2-L3
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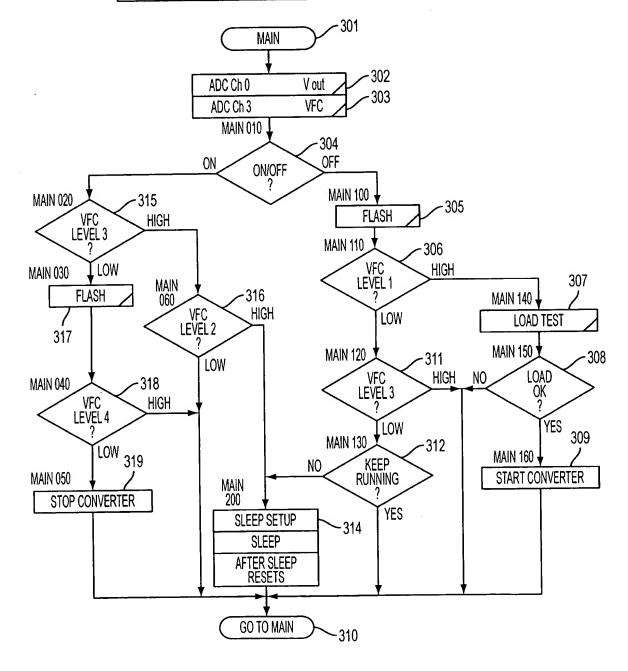


FIG. 6

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SOFTWARE VFC LEVELS

LEVEL 1 - 2.4V IF OFF LOAD TEST ABOVE, WITH WARNING LEVEL 2 - 1.5V IF ON SLEEP ABOVE LEVEL 3 - 1.2V IF ON WARNING BELOW LEVEL 4 - 1.1V IF ON STOP BELOW

HARDWARE TRIP FROM SLEEP IS BETWEEN L2-L3
```

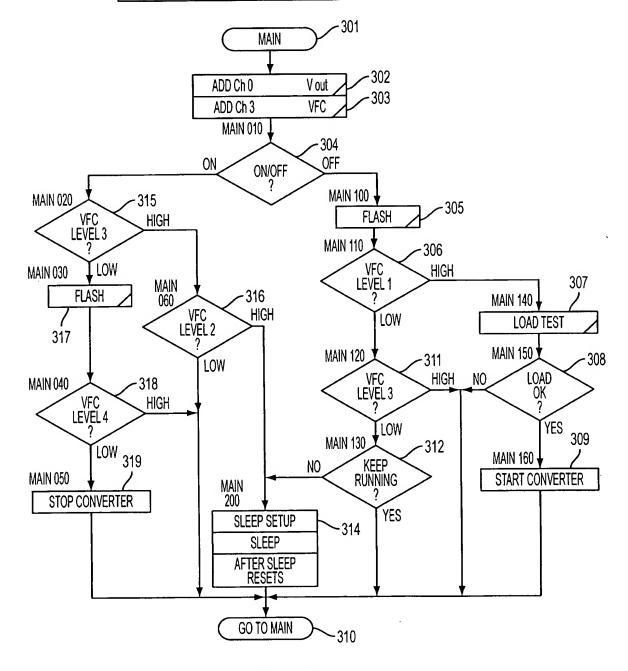


FIG. 7A

FIG. 7B

MAIN:	reti ; Main Program start	; ADC	; ADC Conversion handler
	read adc Ch for SVco ldi ldi rcall	base ZH, SVCC ZL,VCCLOWN ADCRUN	; set chanel ; data store pointer ; call ACD Converter
	read adc ch for SVF0 ldi Idi rcall ;ldi ;ldi ;ldi ;ldi ;cbi	ZH, SVFC ZL,VRCBAN ADCRUN VFCBAHIGH,\$O3 VFCBALOW,\$5e VFCLAHIGH,\$02 VFCLALOW,\$ff ddrB,onnot	; set chanel ; data store pointer ; call ACD Converter ; ••• test for VFC ; ••• test for VFC
MAIN010:	; test OFF/ON sbic rjmp	PINB,ONNOT MAIN100	; read ON pin
MAIN020:	; test vfc for level 3 cpi Idi cpc brsh	VFCBALOW,low(LEV TEMP,high(LEVEL3) VFCBAHIGH,TEMP MAIN060	EL3) ; the value is equ or high
MAIN030:	rcall	FLASH	; do flash
MAIN040:	; test vfc for level 4 cpi ldi cpc brsh	VFCBALOW,low(LEV TEMP,high(LEVEL4) VFCBAHIGH,TEMP MAIN	EL4) ; the value is equ or high, loop to
main	; rjmp	MAIN050	; the value is low fall or jump
MAIN050:	; Stop the converter sbi rjmp	PORTB,ONNOT MAIN	; Stop Converter and test led ; loop to main
MAIN060:	; test vfc for level 2 cpi Idi cpc brsh rjmp	VFCBALOW.low(LE\ Temp,high(LEVEL2) VFCBAHIGH, TEMP MAIN200 MAIN	/EL2) ; the value is equ or high ; the value is low fall or jump
MAIN100:	; do flashe rcall	FLASH	; do flash
MAIN110:	; test vfc for level 1 cpi ldi cpc brsh ; rjmp	VFCBALOW,low(LE' TEMP,high(LEVEL1) VFCBAHIGH,TEMP MAIN140 MAIN120	/EL1) ; the value is equ or high ; the value is low fall or jump
MAIN120:	; test vfc for level 3 cpi VFCBAL ldi TEMP,hic cpc VFCBAH	OW, low(LEVEL3) h(LEVEL3) IGH,TEMP	FIG. 70

	brsh	MAIN	; the value is equ or high
	; rjmp	MAIN130	; the value is low fall or jump
MAIN130:	; test Flasher for stop cpi breq rjmp	eg Flashhigh, Stope Main200 Main	D ; we need to sleep ; keep logging
MAIN140:	; do load test rcall	LOADTEST	; test the load
MAIN150:	; Test for Load OK tst breq	LOADOK MAIN	; go to main
MAIN160:	; start the converter cbi ctr ctr	PORTB, ONNOT FLASHLOW FLASHHIGH	; Start Converter ; Stop Flashing
	rjmp	MAIN	; keep looping
MAIN200:	; enter sleep mode cbi clr clr	ADCSR, ADEN TICA TICB	; Power down the ADC
	idi out	TEMP, 0 TIMSK, TEMP	; stop timer int
	ldi out	TEMP, MCUCRSET MCUCR, TEMP	; set for idel
	; may have to stop tir ;sbi	mers adc intrrupts ddrb, led	,******
	sleep ;cbi	; wate COMPARE ddrb, led	, ***** ,
MAIN210:	; nop ; nop ; rjmp	MAIN210	; we will wate to hear for a low level 2
transet	ldi out	TEMP, TIMSKSET TIMSK, TEMP	; Enable timer int
	sbi rjmp	ADSCR, ADEN MAIN	; Power up the ADC ; back to looping
; Place init code hear	01 - 0 1		
RESET:	; Clear Requesters dr Idi st	r0 z1,29 z,r0	; Clear a master ; Point to req r29 ; Clear
RESET01:	dec z1 brne	; set for next RESET01	; loop
	Setup the ADC Idi out sbi	TEMP, ADCSRSET ADCSR, TEMP ADCSR, ADEN	; Power up the ADC
	: Setup the comparit Idi out	or TEMP, ACSRSET ACSR, TEMP	
	Setup timer 0 for d	iv 64 TEMP, TCCR0SET	FIG. 7D

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	out	TCCR0, TEMP	
	: Setup Timer 1 for 1 ldi out ldi out	.ms int TRMP, TCCR1SET TCCR1, TEMP TEMP, OCR1ASET OCR1A, TEMP	
	: Setup Port B ldi out ldi out	TEMP, DDRBSET DDRB, TEMP TEMP, PORTBSET PORTB, TEMP	; Data direction
	; ldi	ticb, 100	
	: Enable Interrupts Idi out Idi out Idi out	TEMP, TIMSKSET TIMSK, TEMP TEMP, GIMSKSET GIMSK, TEMP TEMP, SREGSET SREG, TEMP	; Enable timer int ; Set the mask ; Enable
	; Setup sleep ldi out	TEMP, MCUCRSET MCUCR, TEMP	
	; setup start delays İdi İdi	TICA, FLASHDEL TICB, LOADDEL	; flash start delay ; load start delay
RESETEND:	rjmp	MAIN	
; This ISR will dec the Time regesters tica and ticb to 0 TIM1_CMP:			
Tic01:	in tst breq dec tst breq	TEMPF, SREG tica tic01 tica ticb tic02	; save status
Tic02:	dec out reti	ticb SREG, TEMPF	; Restor status
; This ISR will handal end of time 0 overflows TIMO_OVF:	; we ret at vector reti		
; This ISR will handal changes in FC Volts it will retern ANA_COMP:	to last place		
ANA_COMIT.	•	fix timer for fast service i	n main
ADC:	reti reti		
EE_RDY	reti		; This ISR may be used
later TIM1_OVF:	reti		; This ISR will be
disabled			FIG 7

FIG. 7E

Rutine to manage low fuel flasher The two byte flash count also acts as a run flag as follow Low byte not 0, the counter is active Low byte equ 0, the high byte has	vs: we and flashing meaning as follws: 0 = clear to start flash 1 = flash time comple!	ing t	
1	any other go to sleep		
FLASH:	; Start Flasher		
	tst brne Idi	TICA FLASHEND TICA, TICFLASH	test for time to run must be zero th run reset the timer
	tst bme tst brne	Flashlow Flash10 FlashHigh Flashend	; test for need ; go to flashing ; test for stoped ; the flasher is stoped
	; Start the flasher Idi Idi	FLASHLOW, LOW(FL FLASHHIGH, HIGH(F	
FLASH10:	; flash the LED cbi	PORTB, LED	; LED lamp on
	; time the flash Idi rcall	TEMP, TIME40m WATE ; I	; load time value wate for time
	;out ;ldi ;out ;sleep	TCNT0, TEMP TEMP, MCUCRSET MCUCR, TEMP	; set for idel
	: stop the flash sbj	PORTB, LED	; LED lamp off
	; count the flashes inc	FLASHLOW FLASHEND	; Adjust Count
	brne inc inc	FLASHLOW FLASHHIGH	; Can not be zero ; Adjust high byte
	brne cIr inc	FLASHEND FLASHLOW FLASHHIGH	; Flash time is over stop flash ; Set stoped
FLASHEND:	ret		
ADCRUN:	rutine for ADC ldi add	TEMP, ADMUXSET TEMP ZH ADMUX, TEMP	
	out sbi ;ldi :aut	ADMUX, 1EMP ADCSR, ADSC TEMP, MCUCRADO MCUCR, TEMP	; Set adc chanel ; Start the ADC Conversion ; set for ADC
ADCRUN01:	;out ;sleep sbis rjmp in st	ADCSR, ADIF ADCRUN01 TEMP, ADCL Z, TEMP ZL	; wate for adc end ; Test for end of conversion ; Loop till end ; Get the resulats
FIG. 7F	inc in st	ZL TEMP, ADCH Z, TEMP	; Get the resulats

LOADTEST:	ret clr ; work load test	LOADOK	; make load not OK	
	tst bme Idi	TICB LOADTESTEND TICB, TICLOAD	; test for time to run ; must be zero th run ; reset the timer	
	sbi	DDRB, LOAD	; start Load by seting output	
	time the load Idi rcall	TEMP, TIME20m WATE	; load timer to start	
	;out ;Idi ;out ;sleep	TCNTO, TEMP TEMP, MCUCRSET MCUCR, TEMP ; wate for time	; set for idel	
	read adc ch for SVFC			
	ldi Idi rcall	ZH, SVFC ZL, VFCLAN ADCRUN	; set chanel ; data store pointer	
	cbi	DDRB, LOAD	; stop Load by try stating	
	; find load dif mov mov sub sbc	VFCDIFHIGH, VFCE	CDIFLOW, VFCBALOW CDIFHIGH, VFCBAHIGH CDIFLOW, VFCLALOW CDIFHIGH, VFCLAGHIGH	
	; test dif cpi Idi cpc brsh	VFCDIFLOW, low(loaddelta) TEMP, high(loaddelta) VFCDIFHIGH, TEMP LOADTESTEND		
LOAD10:	doc	LOADOK	; set load OK \$FF	
LOADTESTEND:	ret			
; runtine to use timer 0 for wating, Temp time				
WATE:				
YVAIL.	out Idi out sleep ret	TCNTO, TEMP TEMP, MCUCRSET MCUCR, TEMP ; wate for time	; set for idel	
Trace:	; A lamp blinb rutin sbic rimp sbi cbi	e for testing PINb, led Tracel PORTb, led PORTb, onnot Traceend		
Tracel:	rjmp cbi	PORTb, led		
Traceend:	sbi ret	PORTb, onnot		
EXIT				

FIG. 7G

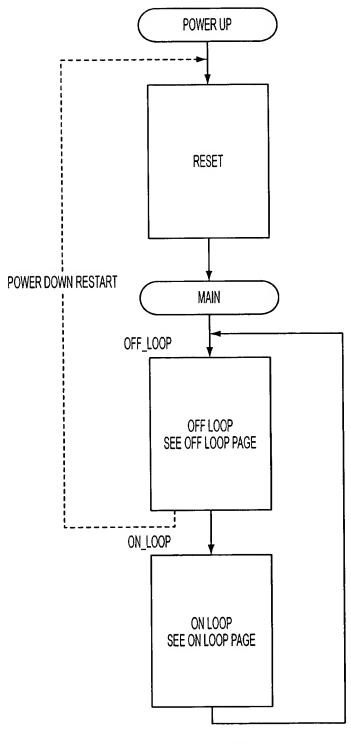


FIG. 8A

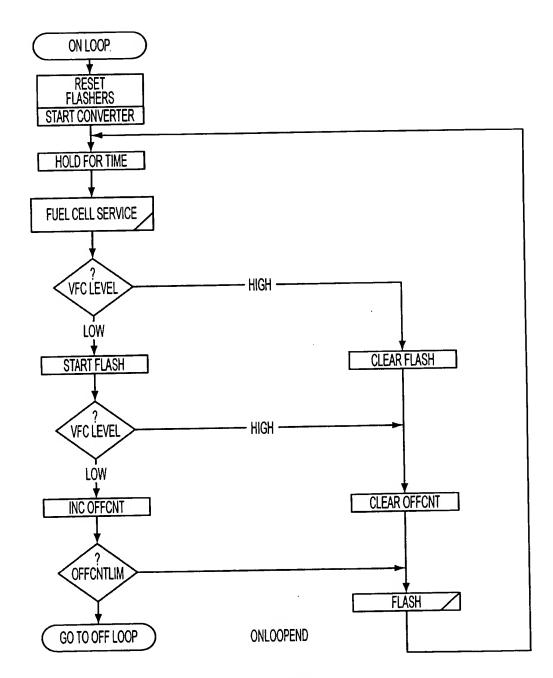


FIG. 8B

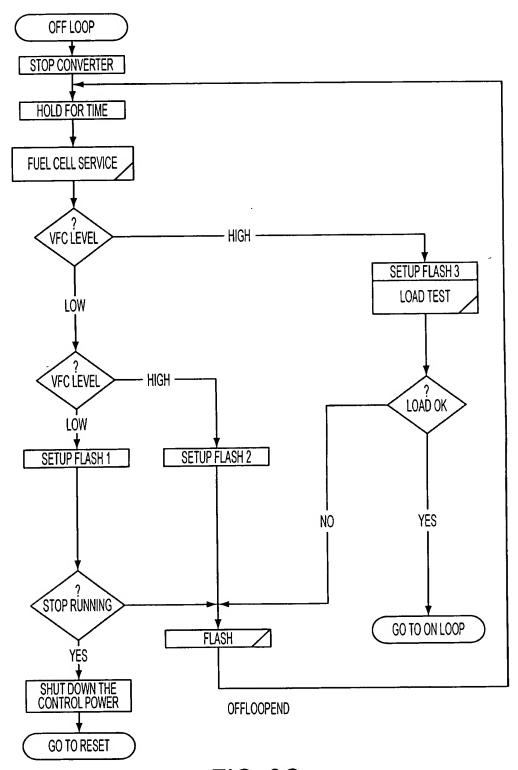


FIG. 8C

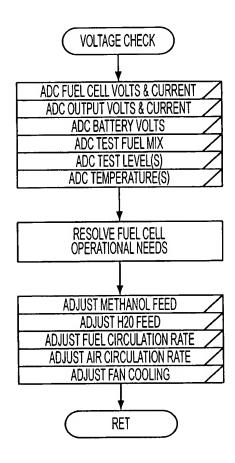
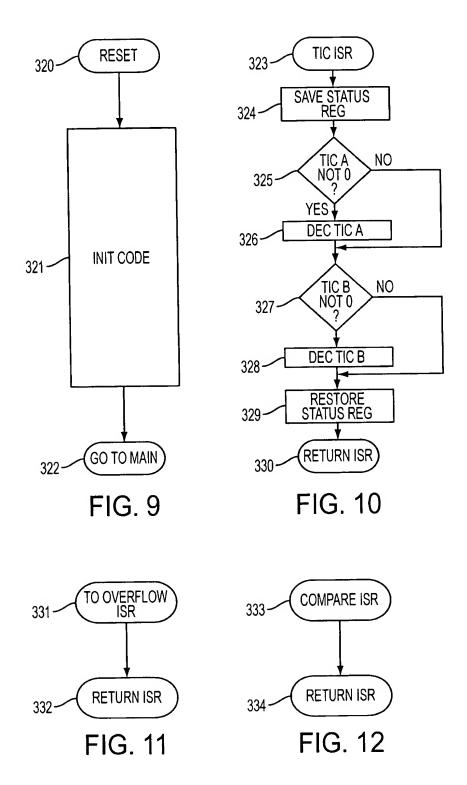
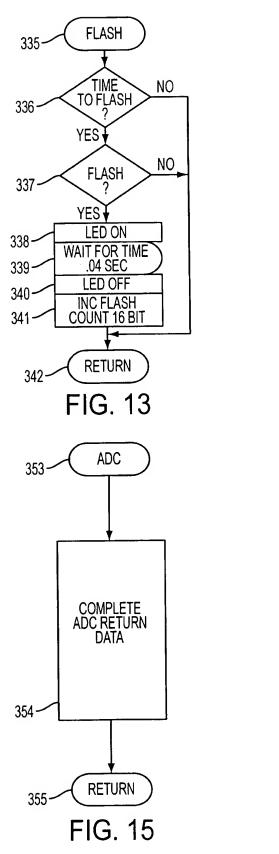
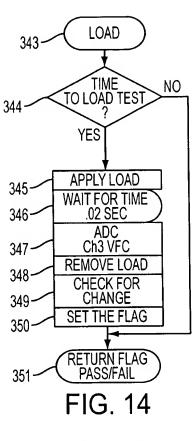
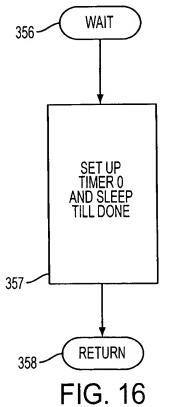


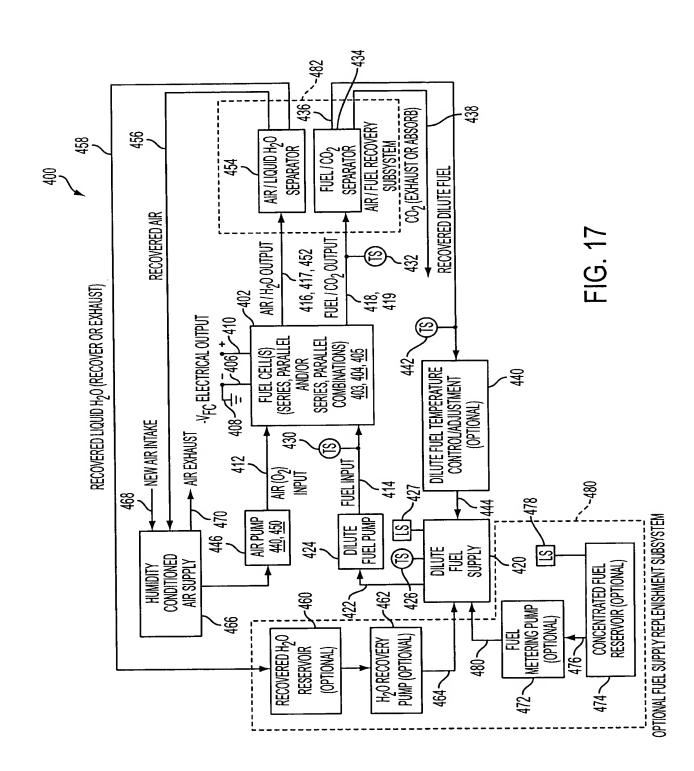
FIG. 8D











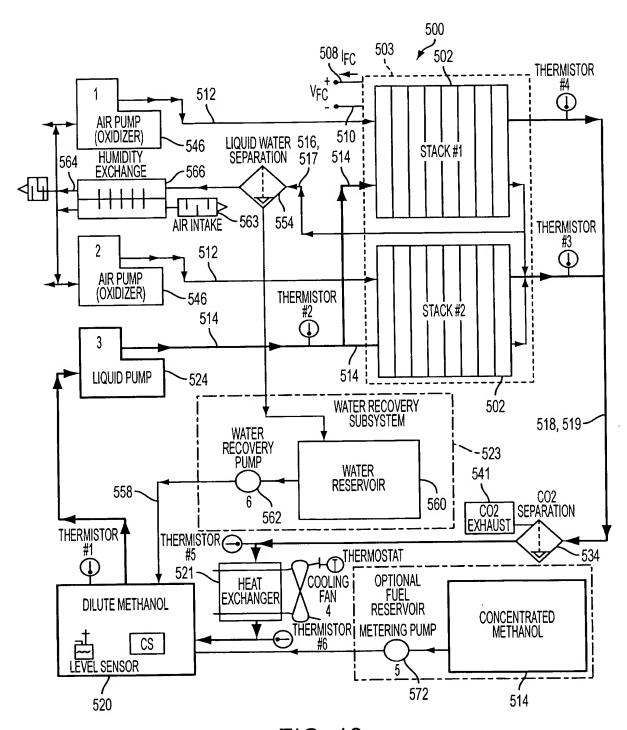


FIG. 18

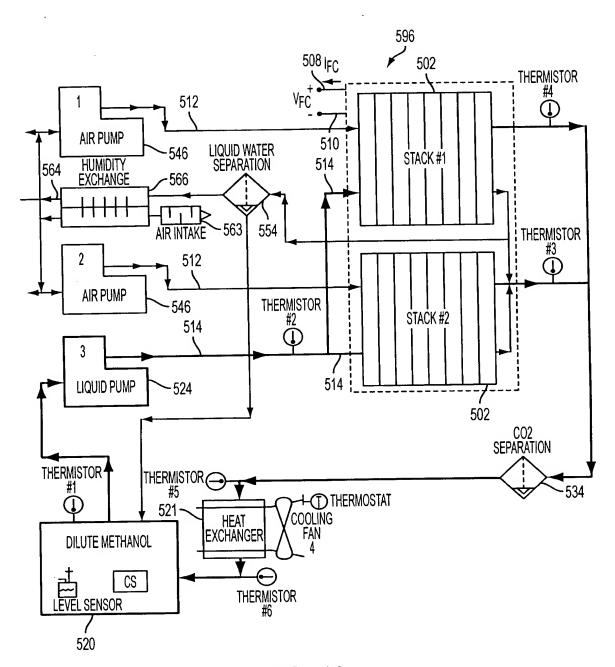


FIG. 19

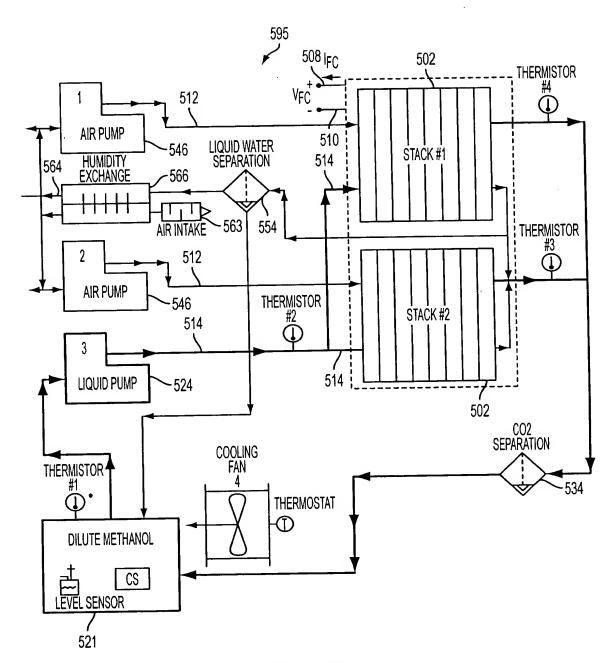


FIG. 20

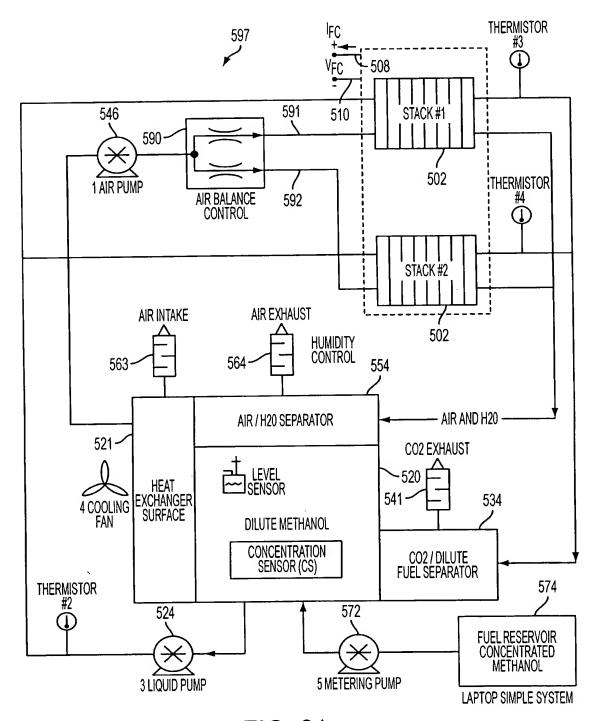
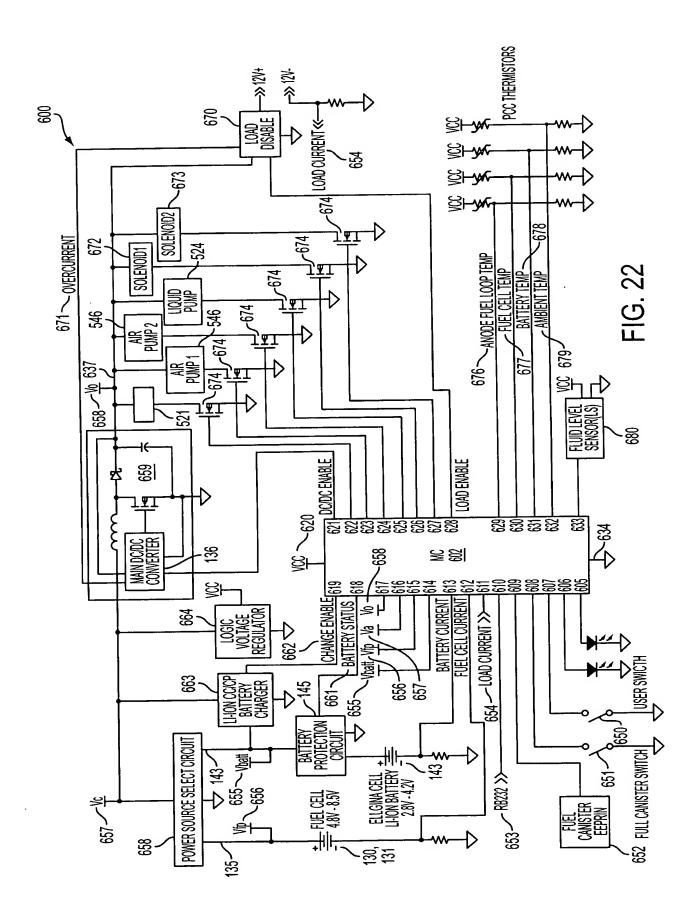
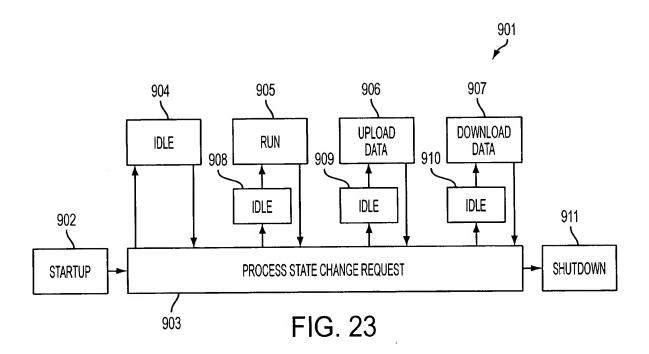


FIG. 21





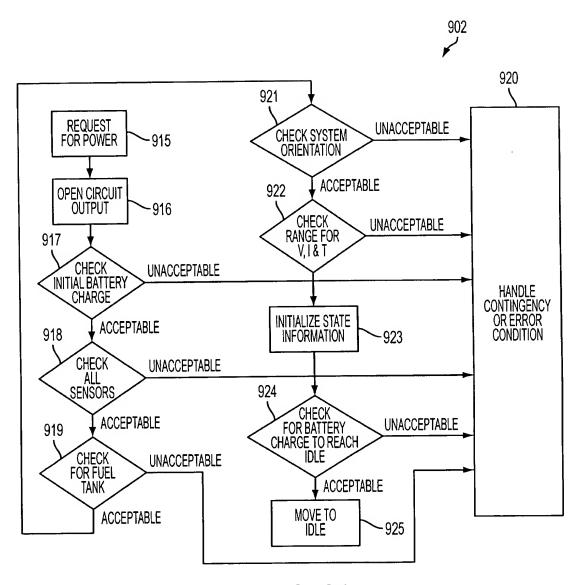


FIG. 24

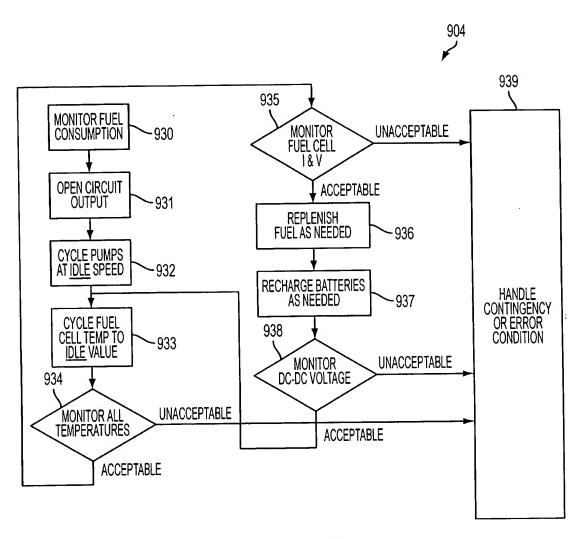


FIG. 25

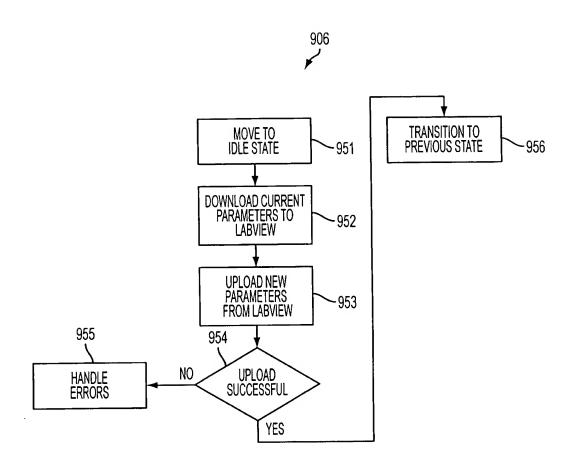


FIG. 26

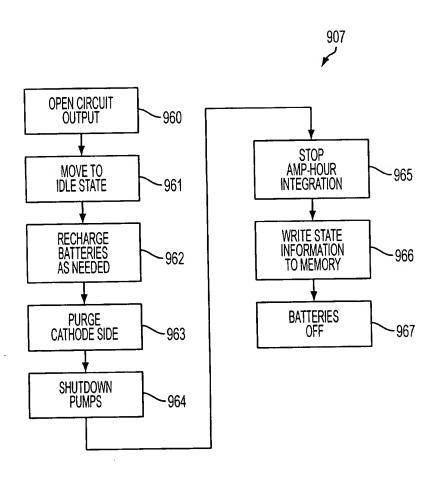


FIG. 27

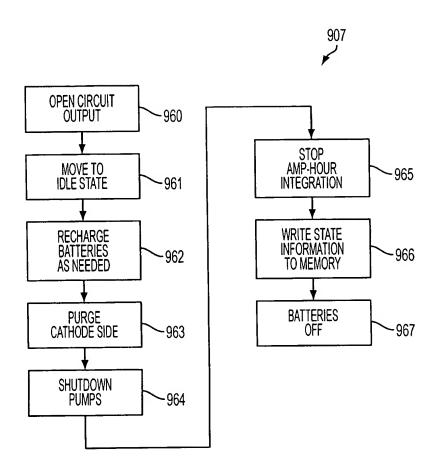


FIG. 28

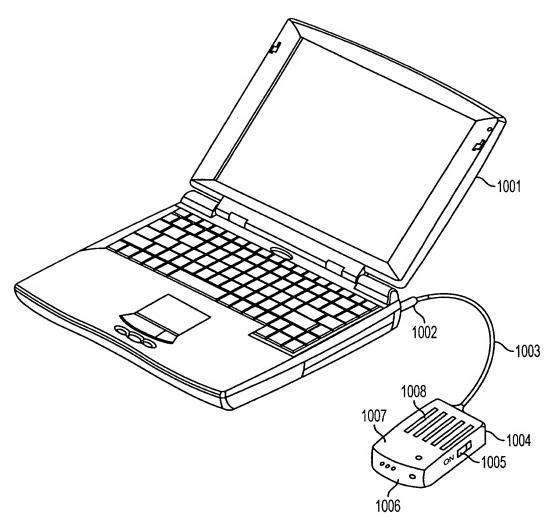


FIG. 29